AN2118
Application note

STLC3075 single supply SLIC for WLL application in buck-boost configuration

Introduction

The STLC3075 is a SLIC device specially designed for WLL (Wireless Local Loop) and ISDN terminal adapters.

This document contains a description of the device functions in buck-boost configuration, and provides some application hints. The device data sheet is an essential complement to this application note, providing important reference information that will simplify understanding of the content.

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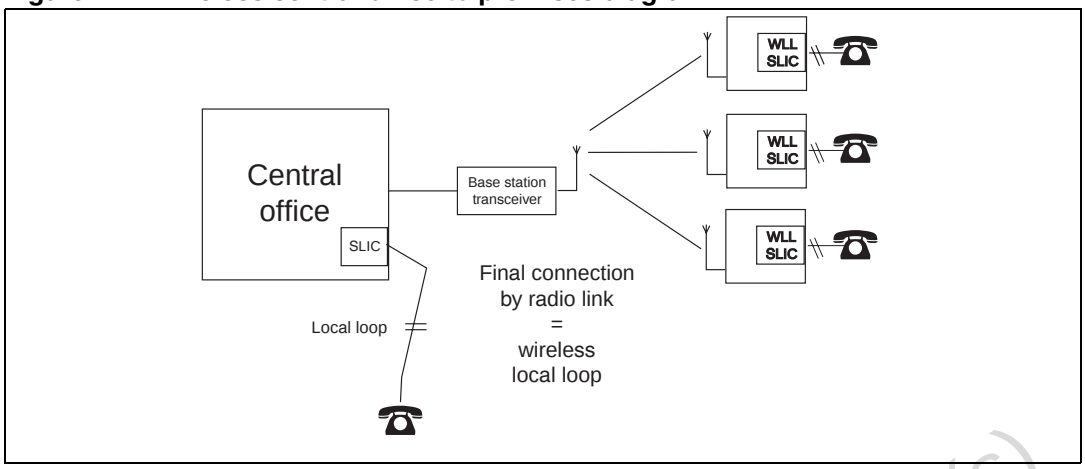
1 Wireless local loop system

Figure 1. Wireless central office to premises diagram



The main characteristics of this device consist in the capability to:

- operate with a single supply voltage in **Buck-Boost** or **Fly-Back** configuration (see AN2132 for information on Fly-Back configuration).
- In **Buck-Boost** configuration, it can operate as in the standard STLC3055N application, with a VPOS voltage in a range from +5.5 V to +12 V.
- generate negative battery voltage
- generate a ring signal (trapezoidal wave form)

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2 Packaging

The STLC3075 is housed in standard TQFP package plastic with copper lead frame. No copper slugs protrude from the plastic body. STLC3075 uses the “standard” package option.

The thermal resistances, shown in *Table 1* and *Figure 2*, are considered between the junction and the ambient still air, and are calculated or measured in ° C/W.

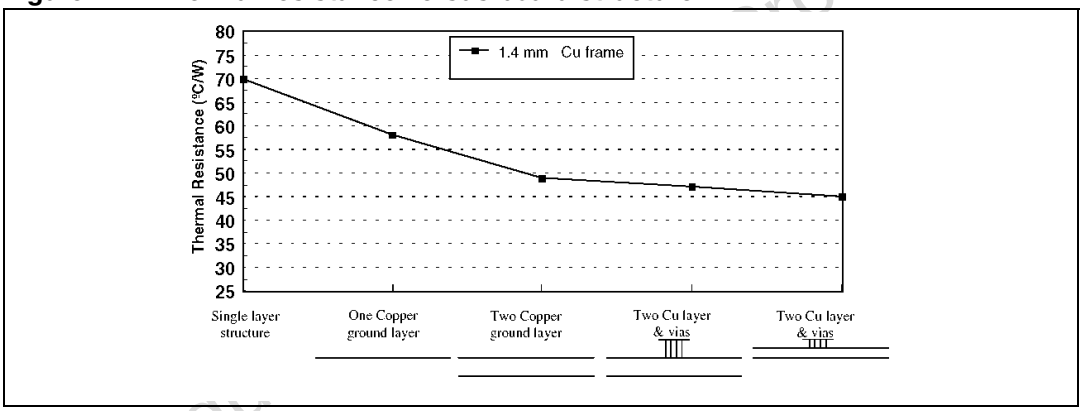
Table 1. Thermal resistance versus package size

Symbol	Parameter	Value	Unit
Rth j-amb	Thermal resistance junction ambient (Full plastic TQFP on single layer board)	70	° C/W
Rth j-amb	Thermal resistance junction ambient (Full plastic TQFP on four layer board)	45	° C/W

2.1 TQFP 10 mm x 10 mm x 1.4 mm

Theta (j-a) on boards, in still air.

Figure 2. Thermal resistance versus board structure



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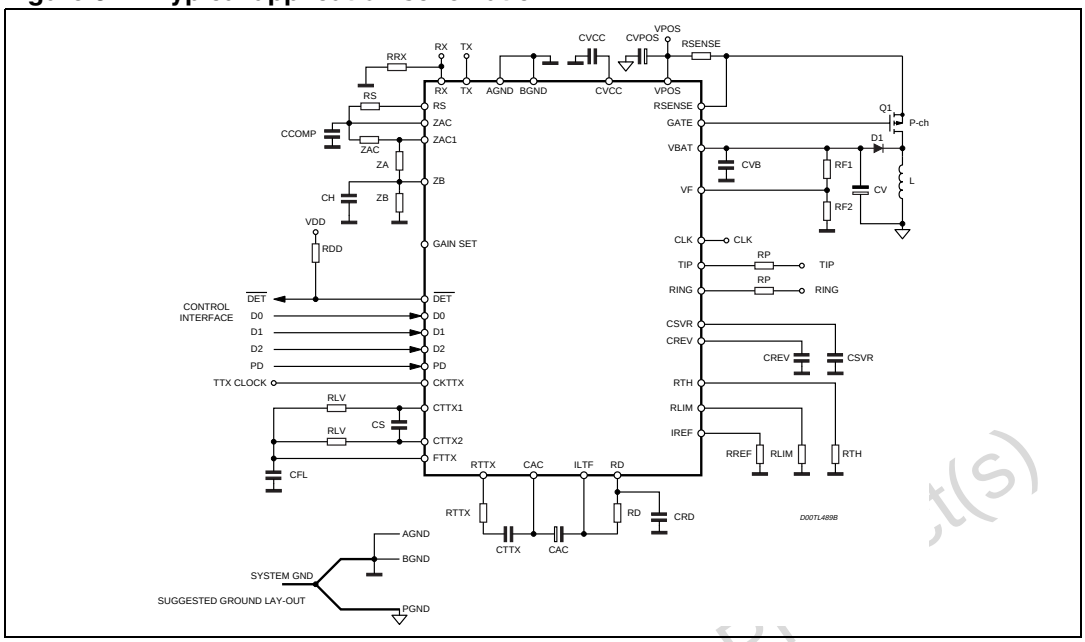
3 Typical application schematic

Figure 3. Typical application schematic



3.1 VBAT voltage generation

When operated with a positive supply voltage VPOS and a correctly set clock signal (typically 125 kHz), the SLIC generates a VBAT voltage for the active and ring operations.

The VBAT voltage level, with a 10% spread, is defined by the voltage divider RF1 / RF2 and can be set by choosing an RF1 value from a recommended set of values (see *Table 2*):

Table 2. VBAT voltage values

RF1 (kΩ)	VBAT (Active mode)	VBAT (Ring mode)
270	-45.8 V	-64.0 V
285	-48.2 V	-67,4 V
300	-51.2 V	-71.8 V
315	-54.0 V	-75.3 V
330	-56.0 V	-78.2 V

These values are referred to the device in active mode, on-hook condition (IL = 0 mA), and in ring mode without load.

The VBAT value must be chosen taking into account the absolute maximum ratings of the device (VBtot = 90 V). VBtot = (VBAT + VPOS) = 90 V must not be exceeded.

When ring mode is selected through the control interface, the VBAT voltage is increased by an internal circuit from it's active level to a predetermined value for ring mode. These two

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voltage levels (VBAT active and VBAT ring) are hence correlated. When one is set, (ring or active), the other is also set at the same time.

3.2 Operation in off-hook condition

A major feature of this device is that when changing from on-hook to off-hook conditions (IL >0 mA), the VBAT voltage is automatically adjusted depending on the loop resistance and on the programmed current limitation value (ILIM).

It should be noted that the device is optimized to operate on short loop applications (RLOOP ≤500 Ω) in order to obtain the correct ring-trip detection.

In these conditions, with line current reaching the programmed constant current feed value (ILIM), the STLC3075 works like a current generator with a fixed DC current.

A fixed voltage drop, 4 V on TIP/GND and approximately 6 V on RING/VBAT, assures the DC functionality and the proper swing for the AC signal.

When the line is set off-hook, the STLC3075 automatically adjusts the generated battery voltage (VBAT) to feed the line with a fixed DC current (programmable via RLIM), and so optimizes power dissipation.

Considering maximum and minimum values for RLOOP ranging from 500 to100 Ω, and with fixed parameters ILIM = 25 mA and 2Rp = 100 Ω, the battery voltage (VBAT) will be equal to:

1. VBAT = 25 mA x (500+100) + 10 V = - 25 V
2. VBAT = 25 mA x (100+100) + 10 V = - 15 V

A correctly set current threshold (typically 9 mA), programmable by external resistor RTH, allows the correct on/off hook transition function.

During the off-hook dynamic transition, the CAC capacitor is charged. The line current regulator system senses the current flowing into RD and reduces the ILOOP current to the programmed ILIM value, set by RLIM.

The settling time of the ILIM current is about 150 ms, and it is a function of the CAC splitter capacitor (min. value allowed is 22 µF).

3.3 VPOS characteristics

The input voltage VPOS can change slowly within the data sheet range (5.5 V - 12 V) without any effect on the VBAT voltage.

The STLC3075 can continue to operate correctly even if the VPOS voltage occasionally goes below 5.5 V (instantaneous value, not steady-state). The only limitation is the minimum voltage required on the external PMOS to keep it in a linear area.

Fast transients, ripples and spikes on the supply voltage V_{POS} will appear on TIP/RING with a reduced amplitude, depending upon the voltage supply rejection of the device.

Bench measurements on SVRR give -35 dB @ f = 50 Hz and -47 dB @ f = 4 kHz, using the test circuit configuration with the device in active mode, loaded with an RLOOP = 500 Ω, and ILIM = 25 mA.

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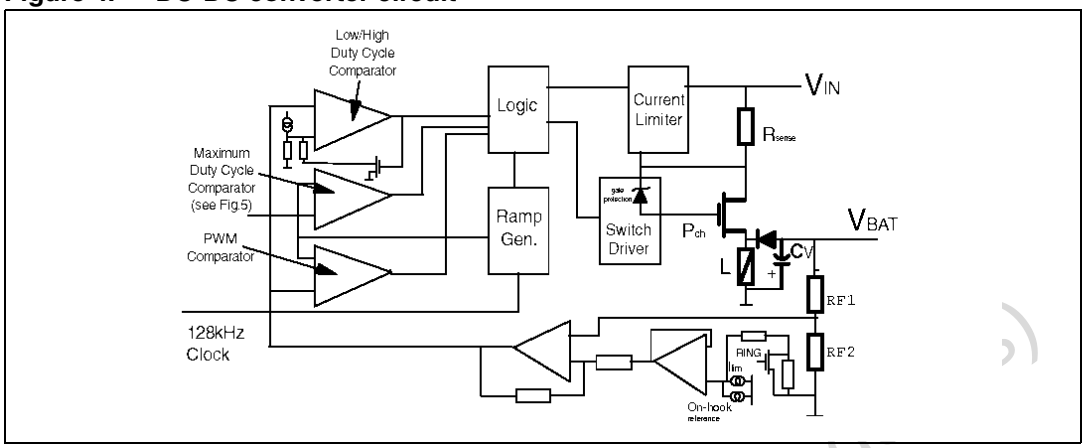
3.4 Start-up and DC-DC converter

In order to prevent problems during start-up, an internal circuit turns-on the gate of the MOSFET only when VPOS reaches 4 V and turns it off for VPOS lower than 3 V.

For VPOS voltage higher than 4 V the DC/DC converter power-on is controlled by a soft start circuit embedded on the devices.

Figure 4. DC-DC converter circuit



The DC\DC converter works in Buck-Boost configuration and its operation can be described as a two step process.

MOSFET in turn-on condition : energy from VPOS is stored in the inductor, diode is reverse biased, and the load on VBAT is powered by the energy stored in the output capacitors CV.

MOSFET in turn-off condition : energy stored in the inductor is delivered to the output capacitor and hence on the load, by the forward biased diode.

An internal circuit controls the duty-cycle of the gate signal so that the output current of the DC\DC converter can be proportional to the load. If a higher power is required for a short time, an embedded circuit fixes the maximum duty-cycle to about 95%. In this case, RSENSE guarantees the maximum value of the limited current.

3.5 Input current limitation

In WLL applications, the power supply usually does not have high-power current capability. Therefore when a ring trip occurs, the status of the SLIC changes from ring mode to off-hook condition. As the loop current control does not react immediately, the line current reaches the output stages current limitation value of about 80 mA. As a consequence, a high peak current is sunk from VPOS which could be higher than its maximum current capability. In this case, if no limiting current circuit is used, (RSENSE = 0), the VPOS voltage would drop.

To prevent this, the STLC3075 incorporates a circuit to limit peak current on the VPOS input. The peak current value is defined by the formula:

$$IPEAK = \frac{100mV}{RSENSE}$$

This input current limitation circuit operates during all transients caused by changes in the line current conditions.

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3.6 VPOS current capability

The table below summarizes the value of the current drawn from VPOS supply vs. REN @ 20 Hz conditions. (For REN definition see *Section 3.9*.)

Table 3. Ivpos average current

VPOS (V)	1REN (Europe)	3REN (Europe)	5REN (USA)
	Ivpos (mA Tot)	Ivpos (mA Tot)	Ivpos (mA Tot)
5.5	130	420	590
6.0	120	280	520
9.0	90	180	360
12.0	60	140	270

When the power supply voltage cannot feed the maximum current (that is, it hasn't got enough current capability), the VPOS voltage will be impacted.

3.7 RSENSE settings

The RSENSE resistor sets the input peak current value, which must be lower than the power supply current capability limit.

In a typical application, the input peak current is fixed at 900 mApK (100 mV / 110 mΩ) in order to guarantee optimum performance in the total range of the current loop (20 to 40 mA) and the VPOS supply (5.5 to 12 V), driving up to 3REN of load.

If the device has to drive up to 5REN, the value of RSENSE must be reduced to between 100 and 90 mΩ. This increases the input peak current to between 1 Apk and 1.1 Apk, which guarantees correct operation at low VPOS voltage conditions (5.5 to 6 V) using a ringing frequency of 20 to 25 Hz.

If the device has to work with a limited input peak current of about 0.6 Apk, setting the RSENSE resistor value in the range of 170 to 180 mΩ, it is mandatory to use a VPOS voltage of 12 V.

3.8 Trapezoidal ringing signal

In the application domain targeted for this product (Integrated Access Device, Set Top Box, Small Office Home Office etc...) non sinusoidal ring waveforms are accepted. Therefore the STLC3075 generates ringing signals with a trapezoidal waveform.

This type of waveform is very similar to a sine wave whose distortion can be kept lower than 5% and crest factors have a value of 1.2, just by correct selection of the external CREV capacitor.

Because the value of CREV is a function of the ringing frequency, this value has to be adapted to the ringing frequency used.

A CREV in the range 18 to 22 nF gives a trapezoidal ringing signal and correct shaping with 20 to 25 Hz ringing frequency. To increase the ringing frequency to 68 Hz, the value of CREV should be chosen in the range of 6.8 to 8.2 nF.

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3.9 Ringer load

3.9.1 With European REN

In a typical application the STLC3075 can drive up to 3REN european standard (1REN = 1800 Ω + 1 µF), @ f = 20 Hz, with crest factor (VppK / Vrms) = 1.22. The levels measured at the ringer terminal are summarized in the following tables.

Table 4. Ringer load (VPOS = 6 V) with European REN

CREV	Crest factor	1 REN		3 REN	
		Vppk	Vrms	Vppk	Vrms
22nF	1.22	62.5V	51.2V	61.8V	50.2V

Table 5. Ringer load (VPOS = 12 V) with European REN

CREV	Crest factor	1 REN		3 REN	
		Vppk	Vrms	Vppk	Vrms
22nF	1.22	63.2V	51.8V	62.8V	50.8V

3.9.2 With USA REN

If the device has to drive up to 5REN, as requested by USA specifications (1REN = 8 µF + 6930 Ω), it is necessary to modify some external components as follows:

RSENSE = 90 mΩ to increase the current capability in order to guarantee this performance @ VPOS = 5.5 V.

RD = 2.2 kΩ in order to avoid false off-hook detection (IRTH = 100 / RD).

The following tables summarize the results @ 20 Hz ringing frequency:

Table 6. Ringer load (VPOS= 6 V) with USA REN

CREV	Crest factor	1 REN		3 REN		5 REN	
		Vppk	Vrms	Vppk	Vrms	Vppk	Vrms
22nF	1.22	62.0V	50.6V	59.6V	48.7V	57.8V	47.0V

Table 7. Ringer load (VPOS=12 V) with USA REN

CREV	Crest factor	1 REN		3 REN		5 REN	
		Vppk	Vrms	Vppk	Vrms	Vppk	Vrms
22nF	1.22	63.0V	51.3V	60.8V	49.3V	58.6V	47.5V

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3.10 Functioning at low VPOS (5.5 V)

When the device is working to VPOS = 5.5 V, good efficiency can be reached if the P-MOS works in the linear region with a series resistance equal to Ron. This gives a proper ID current with Vgs (about VPOS) generated by the driver.

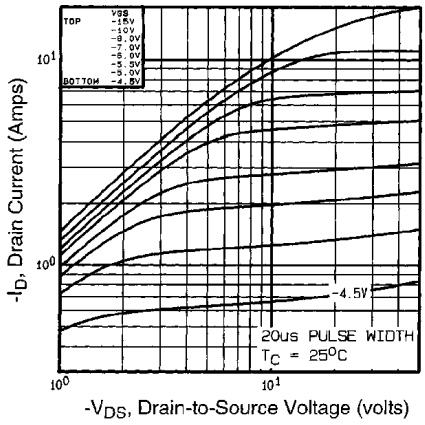
The IRF9510S assures the correct operation in a linear region starting from a minimum VPOS voltage of 5.5 V.

Figure 5 shows that the MOSFET can guarantee a minimum current value of 700 mA with a Vthmax = 4 V, in the condition of Vgs = 5 V and Vds = 1 V.

In the application Vgs = VPOS. Considering the RSENSE drop to be negligible, the value of Vgs-Vth = 1.5 V allows to the MOSFET to work in a linear region.

Linear region is obtained for Vds < Vgs-Vth.

Figure 5. Typical output characteristics Tcase = 25°C



3.11 Efficiency and power dissipation

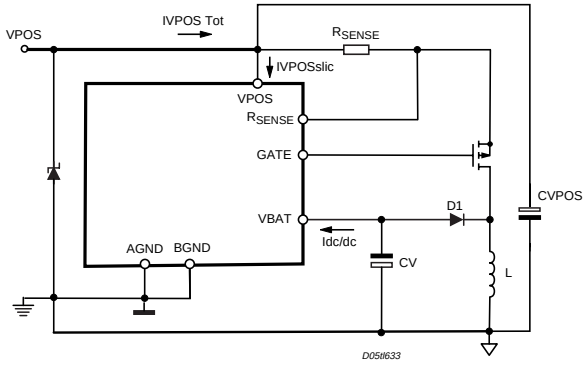
At the fixed CLK frequency, the best DC/DC converter efficiency can be obtained with:

- a good compromise between RDS(ON) and the parasitic input/output capacitances value of the PchMOSFET. For this reason the IRF9510/20 has been chosen (VDSS = -100 V, RDS(ON) =1.2 Ω, ID = -4.0 A).
- a coil inductor for DC/DC applications, like the SMD coil made by Sumida (type CDRH125, 100 µH), with a high efficiency fast recovery diode like the SMBYW01-200 showing a Trr max=35 ns @ VF = 1 A.

Note: *Note that efficiency (η) is also influenced by the value of VPOS.*

Table 8 and *Table 9* summarize the measurements of the DC/DC converter efficiency, made on an ST board.

Figure 6. Circuit configuration for DC/DC converter efficiency measurements



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The efficiency parameter η is calculated with the following formula:

$$\eta = \frac{\frac{Idc}{dc} \cdot VBAT}{IVPOStot - IVPOSslic} \cdot VPOS$$

Measurement conditions:

- external switch PchMOS IRF9510
- SLIC status considered: High impedance; Active with ILOOP=25 mA, RLOOP = 500 Ω
- SMD power inductor, SUMIDA, type CDRH125, typical value 100 µH, Rs = 2.5 Ω, permissible DC current 1.3 A.

Table 8. H.I. feeding @ open circuit

CREV	Crest factor	1 REN Vppk Vrms	3 REN Vppk Vrms	5 REN Vppk Vrms	CREV	Crest factor
6	13.15	3.75	0.17	-50.80	56.40	8.6
12	17.70	4.40	0.20	-51.20	160.00	10.25

Table 9. Active mode @ RLOOP = 500 ohms

VPOS (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	Idc/dc (mA)	Vbat (V)	Pvpos (mW)	Pvbat (mW)	Eff (%)
5.5	177	7.0	29.5	24.8	935.00	731.60	78%
6	160	7.2	29.5	24.8	916.80	731.60	80%
9	111	8.0	29.8	24.8	927.00	739.04	80%
12	86	8.3	29.8	24.8	932.40	739.04	79%

For a given value of supply voltage VPOS, the current consumption from the VPOS supply will be influenced by the electrical characteristics of the selected coil

In order to highlight the power consumption advantages of the STLC3075 compared to the first generation product STLC3055Q, *Table 10* details the H.I. feeding @ open circuit measurements for that first generation device.

Table 10. STLC3055Q H.I. feeding @ open circuit

VPOS (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	Idc/dc (mA)	Vbat (V)	Pvpos (mW)	Pvbat (mW)
6	32	4.6	2.3	-52.2	164.4	120.0
12	22	4.6	2.5	-52.7	208.8	131.7

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3.12 Micro interface

The input levels are interpreted as TTL levels, therefore both 3.3 or 5 V CMOS input signals can be accepted by the STLC3075.

The output DET signal is an open drain (needing an external pull-up resistor to VCC), therefore both 3.3 and 5 V logic levels can be generated, depending on the value of VCC.

3.13 Protection

Different circuit configurations can be used to protect the device from overvoltages.

The best solution to use depends on the specified overvoltage and on whether or not the environment where the STLC3075 has to work is defined by the K20 requirements.

If K20 is requested, a solution that includes a transient voltage suppressor LCP1521, PTC resistors, and two transils has to be used (see *Figure 7*).

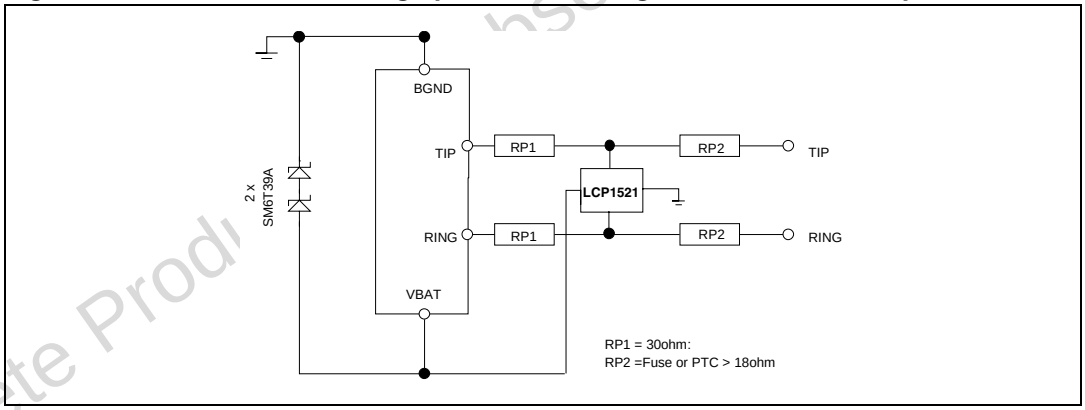
Two diodes inside the LCP1521 will clamp to ground any positive lightning, power cross and voltage overstress.

For negative overvoltages, the device will fire because of the gate triggered on the voltage VBAT. A series of two transils (2 x SM6T39A), to best fit the voltage clamp (typically 78 V), will avoid exceeding the total voltage (Vbtot) applied to the device supply pins.

Note: Vbtot = VPOS + VBAT = 90V according to the absolute maximum rating of the STLC3075.

PTC resistors like the Raychem TR250/80T series will prevent damaging during power cross conditions.

Figure 7. Standard overvoltage protection configuration for K20 compliance



RP1 = 30 Ω and RP2 ≥18 Ω

When K20 requirements are not necessary, a simpler solution consists in the adoption of diodes between VBAT/TIP, RING, TIP, and RING/GND. Suggested diodes are:

- BYT 11-600 or BYW 100-200 for through hole assembly
- STTB 106U or STPR 120A for SMD assembly.

Also in this case, 2 x SM6T39A transils must be used (see *Figure 8*).

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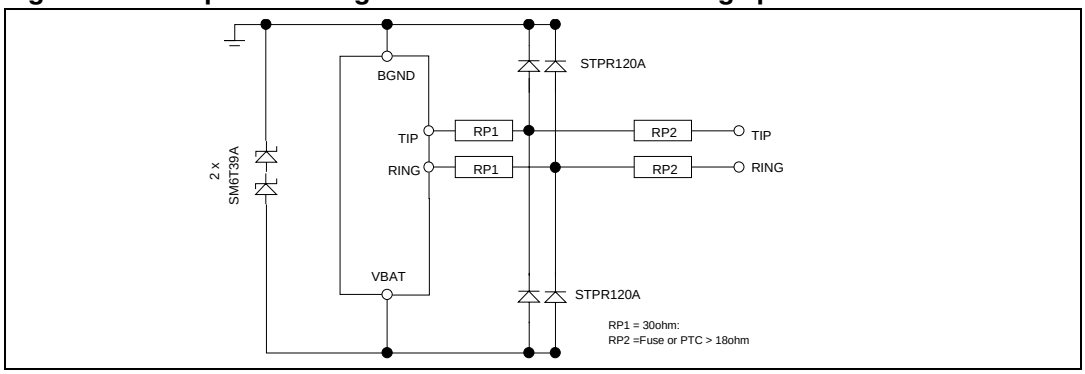
Figure 8. Simplified configuration for indoor overvoltage protection



RP1 = 30 Ω and RP2 ≥18 Ω

3.14 Ring trip

In this SLIC, the ring trip detection is performed by sensing the average current (an image of the line current) injected in the RD resistor, rectified by a dedicated circuit.

It is then filtered by a CAC capacitor and compared to the internally programmed ring trip threshold (IRTH) by the RD resistor itself. Do not confuse this with the RTH resistor which sets the off-hook threshold for active and H.Z. modes.

If the average of the trapezoidal AC current changes in the transition from higher ring impedance (On-hook condition) to low impedance (Off-hook condition), the voltage on the RD resistor increases.

As soon as this voltage goes over the programmed threshold (IRTH), the ring trip will be detected.

In ring mode there is no DC current into the RD resistor, but only the rectified average current. It is clear that the previously described ring trip method is optimized to operate in short loop (<500 Ω) applications and not in the presence of a very long line.

The ring-trip detection threshold is programmed by the formula: IRTH = 100/RD.

With 20 Hz of ring frequency, CAC=22 µF, and RD=4 kΩ, the pin DET goes low about 100 ms after the off-hook transition.

When the SLIC is in ring mode, the maximum average current depends of the REN load. During normal functioning, this current must be lower than the IRTH threshold.

Typical applications can guarantee up to 3REN of load. By increasing the REN number up to 5REN, the AC load will increase. The average current I can then become higher than IRTH and a ring trip will be detected. It is possible to readjust this situation by reducing the value of RD. Alternatively, increasing the IRTH threshold will also increase the ring trip time.

In summary, the ring trip is a function of:

- the load (REN number)
- the value of the ring trip rectified average threshold current "IRTH"
- the value of the maximum peak current sunk from VPOS "Ipk" - higher the REN number lower the value of RSENSE

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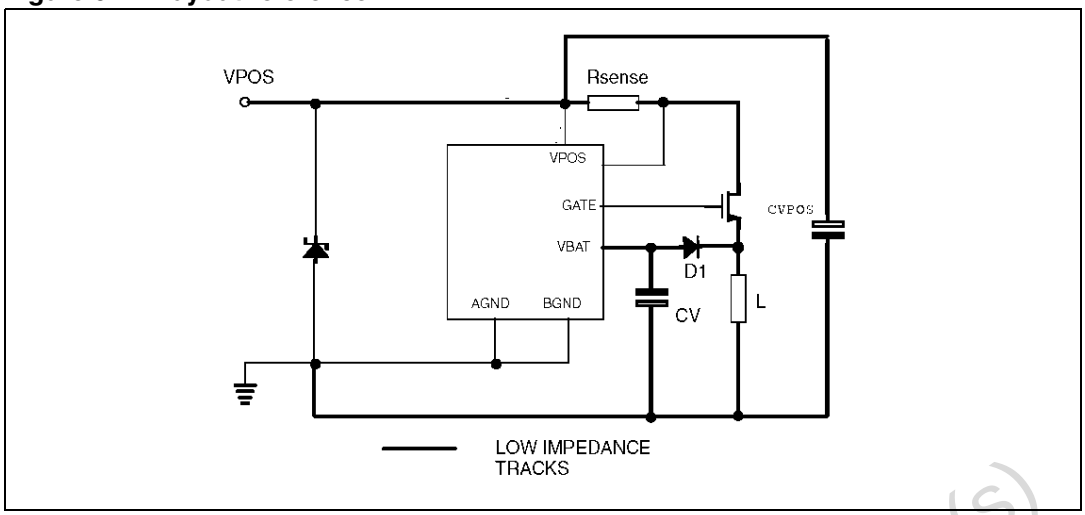
3.15 PCB precautions

Figure 9. Layout reference



Good PCB layout is a basic requirement to avoid noise problems that can have a negative impact on the device operating conditions.

In practice, noise can come from grounding, power supply, parasitic coupling between PCB tracks, and from high impedance points.

The PCB layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (for example: RD, IREF, RTH, RLIM, VF).

As a first recommendation, the components CV, L1, D1,CVPOS, and RSENSE should be kept as close as possible to each other and isolated from the other components.

Noise could be produced by ripple on the CVBAT capacitor and in particular across its equivalent series resistor value (ESR). The lower this value, the lower the ripple that can be present on VBAT.

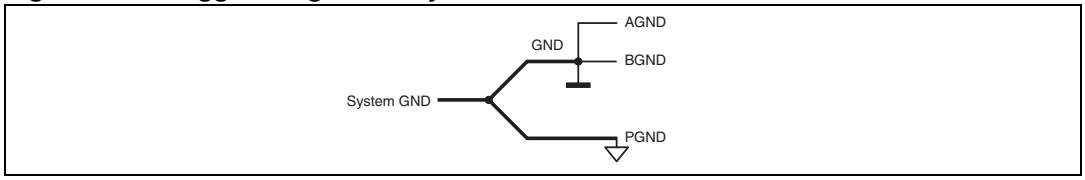
Particular care has to be taken on the tracks used for connection between VPOS and the DC/DC converter, which must be low impedance tracks due to the high current flowing in them.

Noise can also be prevented by connecting RREF (26K1) as close as possible to the IREF pin.

3.16 Ground configuration

Another important point is the ground connection: a star configuration is suggested (see *Figure 10*).

Figure 10. Suggested ground layout



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It is important to create a specific P-GND area on the layout, with connections to:

- the GND of the CV electrolytic capacitor,
- the GND of the CVPOS electrolytic capacitor,
- the GND of the inductor.

This P-GND area has to be connected to the center of the star via a dedicated track.

In this way, any disruptions from the peak current produced by the switching transistor will be cooled by the center of the GND star (system GND), without any disturbance on the other GND (AGND/BGND).

All the other components have to be connected on the GND (AGND/BGND) area.

3.17 Capacitor

Ceramic capacitors CVB and C14 may be used to filter the high frequency ripple and noise that electrolytic capacitors CV and CVPOS respectively are unable to reject.

It is also advisable to connect a 100 nF capacitor from VPOS and GND in order to cancel any high frequency noise on the VPOS pin. This capacitor may not be required, depending on the high frequency sensitivity of the apparatus that the STLC3075 device is included in.

CRD avoids noise coupling on the RD pin, which is a high impedance input.

3.18 On-hook transmission

Voice transmission performances are guaranteed in the complete range of loop currents down to 0 mA, when setting the SLIC in active mode, and receiving data on the RX pin during ringing pause.

The maximum output voltage is correlated to the 2 wires overload voltage parameter (see datasheet).

3.19 Phone detection

The pin DET can also be used to detect the load status of the line.

When the loop is in on-hook condition with a typical telephone connected, setting the SLIC in active reverse polarity and then changing its status to H.I. feeding, pin DET will go to low level for a time of about 1.5 ms. If the line is open, this time is reduced to about 2 µs.

Obsolete Product(s) - Obsolete Product(s)

3.20 ESD immunity

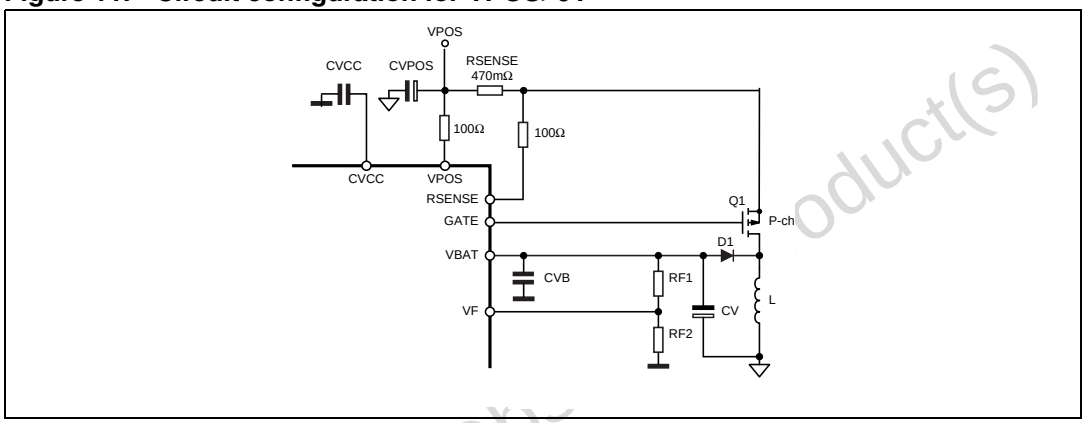
The ESD protection in this device withstands a discharge of 2kV with the Human Body Model. If the STLC3075 must operate in sensitive apparatus where equipment tests against ESD immunity are required (4kV, 8kV), some precautions have be taken.

During these tests, where the device is usually powered, ESD transients can put the internal ESD protection diodes (connected on VPOS and RSENSE pins) into the ON condition.

When the transient disappears and the VPOS supplied is higher than 9 V, the internal ESD diodes are not able to recover back to the OFF condition.

Using a VPOS supply of less than 9 V, the recovery of the ESD diodes is guaranteed and the equipment will be able to pass the ESD immunity tests. When it is not possible to use a reduced VPOS voltage, a solution can be found using the schematic configuration shown in *Figure 11*.

Figure 11. Circuit configuration for VPOS>9V



Since this solution has an impact on the threshold of the input limitation circuit, it is necessary to increase the RSENSE resistor up to 470 mΩ to restore the previous situation.

3.21 Setting resistor

The following current is flowing into the resistor of the STLC3075 application:

- IRLIM, IRTH, IRREF = 1.3 V/R
- IRD = Iline/100
- IRSENSE = 100 mV/RSENSE
- IRF1, IRF2 can be considered around 300 µA
- No DC current flows into RS, ZAC, ZA, ZB, RLV, RTTX.

3.22 Longitudinal balance

To avoid degradation on this parameter, it is very important to use Rp resistors with 1% tolerance, and (if used) PTC resistors with 1% matching.

Low longitudinal balance rejection, caused by the mismatching of the resistors or PTC, can generate noise problems. For example in a GSM based WLL, noise can be generated from the 25 Hz produced by the 4 ms burst of the antenna transmission.

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3.23 TTX filter

A dedicated metering pulse low pass filter (12 kHz to 16 kHz), with 3rd order filtering can be obtained by choosing the following values for the external components:

RLV=16K2//16K2 =8.1K, CFL=1.5 nF, R1=1.3 MΩ, R2=180K, C1=47 pF, C2=6.8 pF.

If the TTX is not requested, the components RLV, CS, CFL, RTTX, CTTX can be removed. In addition, the pins CKTTX, CTTX1, CTTX2, FTTX have to be connected to GND, and the pin RTTX open.

3.24 Gain settings

In order to adapt the SLIC versus the 3.3 V low supply voltage CODEC, the device provides the possibility to change the TX and RX gains by the gain set control pin.

Table 11. Gain settings

Gain set	RX gain	TX gain	Impedance synthesis scale factor
0	0dB	- 6dB	X 50
1	+ 6 dB	- 12dB	X 25

3.25 Complex impedance

Most countries (administration) adopt complex impedance for both the “Exchange Impedance” (Zexch) and the “Balance impedance”, instead of a 600 Ω purely resistive impedance. As a consequence, the AC input impedance that the SLIC plus protection resistor shows at its line terminals (Zs), has to be calculated in order to correctly match the Zexch, to obtain good performance on the return loss parameter.

When Zexch is a complex impedance, the synthesized impedance Zs will be calculated as:

$$Zs = \frac{ZAC}{50} + 2Rp$$

where 50 is a fixed scale factor. (For ZAC definition see datasheet.)

For gain set = 1 the scale factor is 25.

Considering, for example, the ETSI 2 complex impedance Zexch = 270 + (750//150nF)

An AC input impedance has to be synthesized on Pins TIP/RING of the SLIC (ZAC). To do so, considering the line terminal, the correct Zs must be calculated as:

- ZAC=(Zs-2Rp)*50 because 2Rp = 100 Ω
- ZAC= (270-100)*50 + [(750*50)//(150 nF/50)] = ZAC = 8.5K + (37.5K//3 nF)

In this way the SLIC will synthesize Zs impedance matching correctly the Zexch.

Also for the 2 to 4 wire conversion, the administration defines an AC terminal balance impedance Zb properly used to obtain the THL performance.

Good trans-hybrid loss performance, and therefore a proper echo cancellation, can be obtained by correctly matching the two external impedances, ZA and ZB, which can also be complex impedances.

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ZA = 50 x Zexch

ZB = 50 x Zb

For gain set = 1 the scale factor is 25

In the case of Zb=Zexch, the impedances ZA and ZB can be replaced by two resistors calculating their value as:

ZA = ZB = 50 x |Zexch|. For gain set = 1 the scale factor is 25.

Where |Zexch| is the modules @ 1 kHz.

For ETSI 2 the value |Zexch| = 842 Ω

ZA = ZB = 50 x 842 Ω = 42.1 kΩ

A typical value of 120 pF (with gain set = 0) for the capacitors CComp and CH guarantee both loop stability and good THL performance.

For gain set = 1 the capacitor value is doubled.

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4 Support

Please contact your local ST sales office for details of the STLC3075 firmware.

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
15-May-2005	1	Initial release.
15-Nov-2005	2	Modified *Figure 11*.
16-Feb-2007	3	Updated *Figure 3*.

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